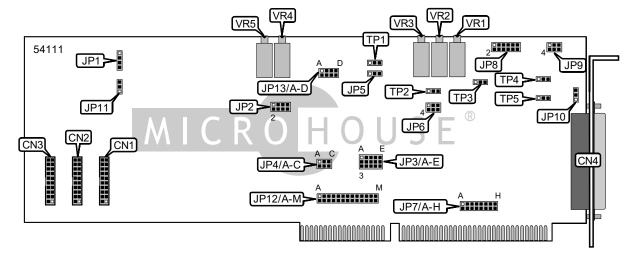
ACQUTEK CORPORATION PA-MA12(-H)

Card TypeData AcquisitionChip SetUnidentifiedMaximum Onboard MemoryUnidentifiedI/O OptionsAnalog input, digital input, digital I/O connectors (3)Data Bus16-bit ISACard SizeFull-length



| CONNECTIONS | | | | | | | |
|---|-------|-------------------------------|-------|--|--|--|--|
| Function | Label | Function | Label | | | | |
| XDI expansion board connector | CN1 | A/D converter CMRR selector | VR1 | | | | |
| XDI expansion board connector | CN2 | A/D converter offset selector | VR2 | | | | |
| XDI expansion board connector | CN3 | A/D converter range selector | VR3 | | | | |
| 37-pin analog/digital signals connector | CN4 | D/A converter range selector | VR4 | | | | |
| Timer signal input (8254) | JP1 | D/A converter offset selector | VR5 | | | | |
| External clock input | JP10 | | | | | | |

| USER CONFIGURABLE SETTINGS | | | | | | |
|----------------------------|-----|--------------------------|--|--|--|--|
| Function Label Position | | | | | | |
| Differential A/D input | JP9 | Pins 1 & 2, 4 & 5 closed | | | | |
| Single ended A/D input | JP9 | Pins 2 & 3, 5 & 6 closed | | | | |

| TESTING JUMPER SETTINGS | | | | | | | |
|-------------------------------------|-------|--------------------------|--|--|--|--|--|
| Function | Label | Position | | | | | |
| í Factory configured - do not alter | JP2 | Pins 1 & 2, 3 & 4 closed | | | | | |
| í Factory configured - do not alter | JP11 | Pins 1 & 2 closed | | | | | |
| í Factory configured - do not alter | TP1 | Pins 1 & 2 closed | | | | | |
| í Factory configured - do not alter | TP2 | Pins 1 & 2 closed | | | | | |
| í Factory configured - do not alter | TP3 | Pins 1 & 2 closed | | | | | |
| í Factory configured - do not alter | TP4 | Pins 1 & 2 closed | | | | | |
| í Factory configured - do not alter | TP5 | Pins 1 & 2 closed | | | | | |

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| DATA TRANSFER SELECTION | | | | | | | |
|---|--------|--------|--------|--|--|--|--|
| Data length | JP4/A | JP4/B | JP4/C | | | | |
| í Automatic Word/Byte data transfer enabled | Open | Closed | Open | | | | |
| Byte data transfer for A/D data (8 bits) | Closed | Open | Open | | | | |
| Word data transfer for A/D data (16 bits) | Open | Open | Closed | | | | |

| DMA CHANNEL SELECTION | | | | | | | | |
|-----------------------|---|----------|----------|----------|----------|----------|----------|--|
| Channel | JP12/A | JP12/B-C | JP12/D-E | JP12/F-G | JP12/H-I | JP12/J-K | JP12/L-M | |
| 0 | Open | Open | Open | Open | Open | Open | Closed | |
| 1 | Open | Open | Open | Open | Open | Closed | Open | |
| 3 | Open | Open | Open | Open | Closed | Open | Open | |
| 5 | Closed | Open | Open | Closed | Open | Open | Open | |
| 6 | Closed | Open | Closed | Open | Open | Open | Open | |
| 7 | Closed | Closed | Open | Open | Open | Open | Open | |
| Note: Channe | Note: Channels 0,5,6, & 7 are not available for PC & PC-XT. | | | | | | | |

| D/A OUTPUT VOLTAGE RANGE SELECTION | | | | | | | |
|------------------------------------|--------|--------|--------|--------|--|--|--|
| Voltage | JP13/A | JP13/B | JP13/C | JP13/D | | | |
| í OV to 5V | Open | Closed | Open | Open | | | |
| 0V to 10V | Open | Open | Closed | Open | | | |
| -5V to 5V | Open | Closed | Open | Closed | | | |
| -10V to 10V | Open | Open | Closed | Closed | | | |

| A/D INPUT VOLTAGE RANGE SELECTION | | | | | | |
|-----------------------------------|-------|--------------------------|--|--|--|--|
| Function | Label | Position | | | | |
| í 5V A/D input | JP5 | Pins 2 & 3 closed | | | | |
| 10V A/D input | JP5 | Pins 1 & 2 closed | | | | |
| í Bipolar A/D input | JP6 | Pins 1 & 2, 4 & 5 closed | | | | |
| Unipolar A/D input | JP6 | Pins 2 & 3, 5 & 6 closed | | | | |

| A/D INPUT GAIN SELECTION | | | | | |
|--------------------------|---------------------|--|--|--|--|
| Gain | JP8 | | | | |
| Not installed | Open | | | | |
| í 1 | Pins 9 & 11 closed | | | | |
| 2 | Pins 11 & 12 closed | | | | |
| 5 | Pins 9 & 10 closed | | | | |
| 10 | Pins 7 & 8 closed | | | | |
| 20 | Pins 5 & 6 closed | | | | |
| 50 | Pins 3 & 4 closed | | | | |
| User defined | Pins 1 & 2 closed | | | | |

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| BASE I/O ADDRESS SELECTION | | | | | | | | |
|----------------------------|---|-------------|---------------|---------------|--------------|---------------|--------------|-------------|
| Setting | JP7/A | JP7/B | JP7/C | JP7/D | JP7/E | JP7/F | JP7/G | JP7/H |
| 000h | Closed | Closed | Closed | Closed | Closed | Closed | Closed | Closed |
| 010h | Closed | Closed | Closed | Closed | Closed | Closed | Closed | Open |
| 020h | Closed | Closed | Closed | Closed | Closed | Closed | Open | Closed |
| 030h | Closed | Closed | Closed | Closed | Closed | Closed | Open | Open |
| 040h | Closed | Closed | Closed | Closed | Closed | Open | Closed | Closed |
| í 2E0h | Closed | Closed | Open | Closed | Open | Open | Open | Closed |
| FB0h | Open | Open | Open | Open | Open | Closed | Open | Open |
| FC0h | Open | Open | Open | Open | Open | Open | Closed | Closed |
| FD0h | Open | Open | Open | Open | Open | Open | Closed | Open |
| FE0h | Open | Open | Open | Open | Open | Open | Open | Closed |
| FF0h | Open | Open | Open | Open | Open | Open | Open | Open |
| Note: | A total of 2 | 56 base add | lress setting | s are availat | ole. The jum | ipers are a b | inary repres | entation of |
| | | | | | | | nd switch JF | |
| | Least Significant Bit. The switches have the following decimal values: JP7/A=2048, | | | | | | | |
| | JP7/B=1024, JP7/C=512, JP7/D=256, JP7/E=128, JP7/F=64, JP7/G=32, JP7/H=16. Turn off | | | | | | | |
| | the switch | es and add | the values | of the swit | ches to obt | tain the cor | rect memor | y address. |
| | (Open=1, 0 | Closed=0) | | | | | | |

| IRQ INTERRUPT SELECTION | | | | | | | | |
|--|------------|------------|------------|------------|------------|--|--|--|
| IRQ | JP3/A | JP3/B | JP3/C | JP3/D | JP3/E | | | |
| IRQ2 | Open | Open | Open | Open | Pins 1 & 2 | | | |
| IRQ3 | Open | Open | Open | Pins 1 & 2 | Open | | | |
| IRQ4 | Open | Open | Pins 1 & 2 | Open | Open | | | |
| í IRQ5 | Open | Pins 1 & 2 | Open | Open | Open | | | |
| IRQ7 | Pins 1 & 2 | Open | Open | Open | Open | | | |
| IRQ10 | Open | Open | Open | Open | Pins 2& 3 | | | |
| IRQ11 | Open | Open | Open | Pins 2& 3 | Open | | | |
| IRQ12 | Open | Open | Pins 2& 3 | Open | Open | | | |
| IRQ14 | Open | Pins 2 & 3 | Open | Open | Open | | | |
| IRQ15 | Pins 2 & 3 | Open | Open | Open | Open | | | |
| Disabled | Open | Open | Open | Open | Open | | | |
| Note: Pins designated are in the closed position. IRQ10, IRQ11, IRQ12, IRQ14 & IRQ15 are for AT compatible buses; PC buses will not support them. | | | | | | | | |