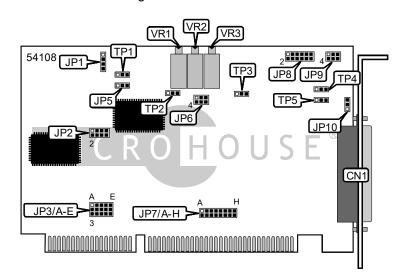
ACQUTEK CORPORATION PA-AD12(-H)

Card Type Data Acquisition
Chip Set None

Maximum Onboard Memory
I/O Options
Data Bus
Card Size

Unidentified
Analog/digital I/O
16-bit ISA
Half-length



CONNECTIONS					
Function	Label	Function	Label		
37-pin analog/digital signals connector	CN1	A/D converter offset selector	VR1		
Timer signal input (8254)	JP1	A/D converter range selector	VR2		
External clock input	JP10	A/D converter CMRR selector	VR3		

USER CONFIGURABLE SETTINGS					
Function	Label	Position			
Differential A/D input	JP9	Pins 1 & 2, 4 & 5 closed			
Single ended A/D input	JP9	Pins 2 & 3, 5 & 6 closed			

TESTING JUMPER SETTINGS						
Function	Label	Position				
í Factory configured - do not alter	JP2	Pins 1 & 2, 3 & 4 closed				
í Factory configured - do not alter (S/H enabled)	TP1	Pins 1 & 2 closed				
í Factory configured - do not alter	TP2	Pins 1 & 2 closed				
í Factory configured - do not alter	TP3	Pins 1 & 2 closed				
í Factory configured - do not alter	TP4	Pins 1 & 2 closed				
í Factory configured - do not alter	TP5	Pins 1 & 2 closed				

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A/D INPUT VOLTAGE RANGE SELECTION						
Function	Label	Position				
í 5V A/D input	JP5	Pins 2 & 3 closed				
10V A/D input	JP5	Pins 1 & 2 closed				
í Bipolar A/D input	JP6	Pins 1 & 2, 4 & 5 closed				
Unipolar A/D input	JP6	Pins 2 & 3, 5 & 6 closed				

A/D INPUT GAIN SELECTION					
Gain	JP8				
Not installed	Open				
í 1	Pins 9 & 11 closed				
2	Pins 11 & 12 closed				
5	Pins 9 & 10 closed				
10	Pins 7 & 8 closed				
20	Pins 5 & 6 closed				
50	Pins 3 & 4 closed				
User defined	Pins 1 & 2 closed				

BASE I/O ADDRESS SELECTION								
Setting	JP7/A	JP7/B	JP7/C	JP7/D	JP7/E	JP7/F	JP7/G	JP7/H
000h	Closed							
010h	Closed	Open						
020h	Closed	Closed	Closed	Closed	Closed	Closed	Open	Closed
030h	Closed	Closed	Closed	Closed	Closed	Closed	Open	Open
040h	Closed	Closed	Closed	Closed	Closed	Open	Closed	Closed
í 2E0h	Closed	Closed	Open	Closed	Open	Open	Open	Closed
FB0h	Open	Open	Open	Open	Open	Closed	Open	Open
FC0h	Open	Open	Open	Open	Open	Open	Closed	Closed
FD0h	Open	Open	Open	Open	Open	Open	Closed	Open
FE0h	Open	Closed						
FF0h	Open							
Note: A total of 256 base address settings are available. The jumpers are a binary representation of								

A total of 256 base address settings are available. The jumpers are a binary representation of the decimal memory addresses. JP7/A is the Most Significant Bit and switch JP7/H is the Least Significant Bit. The switches have the following decimal values: JP7/A=2048, JP7/B=1024, JP7/C=512, JP7/D=256, JP7/E=128, JP7/F=64, JP7/G=32, JP7/H=16. Turn off the switches and add the values of the switches to obtain the correct memory address. (Open=1, Closed=0)

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AQUTEK CORPORATION PA-AD12(-H)

IRQ INTERRUPT SELECTION							
IRQ	JP3/A	JP3/B	JP3/C	JP3/D	JP3/E		
IRQ2	Open	Open	Open	Open	Pins 1 & 2		
IRQ3	Open	Open	Open	Pins 1 & 2	Open		
IRQ4	Open	Open	Pins 1 & 2	Open	Open		
í IRQ5	Open	Pins 1 & 2	Open	Open	Open		
IRQ7	Pins 1 & 2	Open	Open	Open	Open		
IRQ10	Open	Open	Open	Open	Pins 2& 3		
IRQ11	Open	Open	Open	Pins 2& 3	Open		
IRQ12	Open	Open	Pins 2& 3	Open	Open		
IRQ14	Open	Pins 2 & 3	Open	Open	Open		
IRQ15	Pins 2 & 3	Open	Open	Open	Open		
Disabled	Open	Open	Open	Open	Open		

Note: JP3 jumper may be labeled JP3/4 on the board. Pins designated are in the closed position. IRQ10, IRQ11, IRQ12, IRQ14 & IRQ15 are for AT compatible buses; PC buses will not support them.