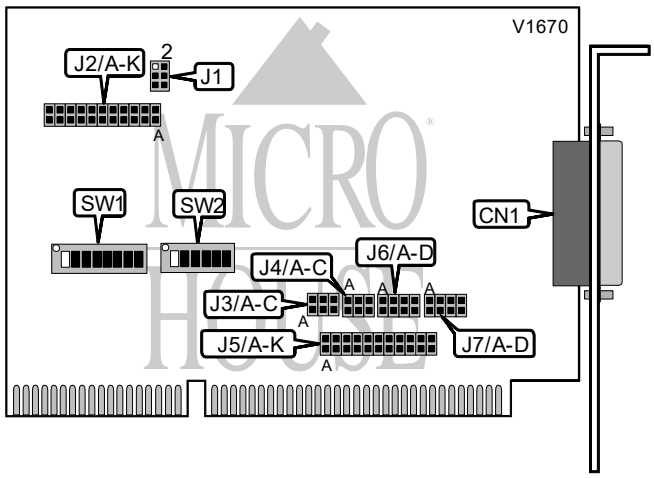
QUATECH, INC.
O C E - 1 0 0

Card Type	Parallel card
Chip Set	Unidentified
Maximum Onboard Memory	None
I/O Options	Parallel ports
Data Bus	16-bit ISA



CONNECTIONS	
Function	Label
Parallel Port	CN1

USER CONFIGURABLE SETTINGS		
Function	Label	Position
í Factory configured - do not alter	J1	Pins 1 & 2, 4 & 5 closed

INTERRUPT SELECTION						
IRQ	J5/A	J5/B	J5/C	J5/D	J5/E	J5/F
Disabled	Open	Open	Open	Open	Open	Open
2/9	Closed	Open	Open	Open	Open	Open
3	Open	Closed	Open	Open	Open	Open
4	Open	Open	Closed	Open	Open	Open
5	Open	Open	Open	Closed	Open	Open
6	Open	Open	Open	Open	Closed	Open
7	Open	Open	Open	Open	Open	Closed
10	Open	Open	Open	Open	Open	Open
11	Open	Open	Open	Open	Open	Open
12	Open	Open	Open	Open	Open	Open
14	Open	Open	Open	Open	Open	Open
15	Open	Open	Open	Open	Open	Open

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INTERRUPT SELECTION (CON'T)					
IRQ	J5/G	J5/H	J5/I	J5/J	J5/K
Disabled	Open	Open	Open	Open	Open
2/9	Open	Open	Open	Open	Open
3	Open	Open	Open	Open	Open
4	Open	Open	Open	Open	Open
5	Open	Open	Open	Open	Open
6	Open	Open	Open	Open	Open
7	Open	Open	Open	Open	Open
10	Closed	Open	Open	Open	Open
11	Open	Closed	Open	Open	Open
12	Open	Open	Closed	Open	Open
14	Open	Open	Open	Closed	Open
15	Open	Open	Open	Open	Closed

DMA CANNEL SLECTION						
DMA	J3/A	J3/B	J3/C	J4/A	J4/B	J4/C
Disabled	Open	Open	Open	Open	Open	Open
0	Open	Open	Open	Open	Open	Open
1	Open	Open	Open	Open	Open	Open
2	Open	Open	Open	Open	Open	Open
3	Open	Open	Open	Open	Open	Open
5	Closed	Open	Open	Closed	Open	Open
6	Open	Closed	Open	Open	Closed	Open
7	Open	Open	Closed	Open	Open	Closed

DMA CANNEL SLECTION (CON'T)								
DMA	J6/A	J6/B	J6/C	J6/D	J7/A	J7/B	J7/C	J7/D
Disabled	Open	Open	Open	Open	Open	Open	Open	Open
0	Closed	Open	Open	Open	Closed	Open	Open	Open
1	Open	Closed	Open	Open	Open	Closed	Open	Open
2	Open	Open	Closed	Open	Open	Open	Closed	Open
3	Open	Open	Open	Closed	Open	Open	Open	Closed
5	Open	Open	Open	Open	Open	Open	Open	Open
6	Open	Open	Open	Open	Open	Open	Open	Open
7	Open	Open	Open	Open	Open	Open	Open	Open

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FASTBYTES PROTOCOL SELECTION						
Setting	J2/A	J2/B	J2/C	J2/D	J2/E	J2/F
0	Closed	Open	Open	Open	Open	Open
1	Open	Closed	Open	Open	Open	Open
2	Open	Open	Closed	Open	Open	Open
3	Open	Open	Open	Closed	Open	Open
4	Open	Open	Open	Open	Closed	Open
5	Open	Open	Open	Open	Open	Closed
6	Open	Open	Open	Open	Open	Open
7	Open	Open	Open	Open	Open	Open
8	Open	Open	Open	Open	Open	Open
9	Open	Open	Open	Open	Open	Open
10	Open	Open	Open	Open	Open	Open

FASTBYTES PROTOCOL SELECTION (CON'T)					
Setting	J2/G	J2/H	J2/I	J2/J	J2/K
0	Open	Open	Open	Open	Open
1	Open	Open	Open	Open	Open
2	Open	Open	Open	Open	Open
3	Open	Open	Open	Open	Open
4	Open	Open	Open	Open	Open
5	Open	Open	Open	Open	Open
6	Closed	Open	Open	Open	Open
7	Open	Closed	Open	Open	Open
8	Open	Open	Closed	Open	Open
9	Open	Open	Open	Closed	Open
10	Open	Open	Open	Open	Closed

BASE I/O ADDRESS SELECTION								
Setting	SW1/1	SW1/2	SW1/3	SW1/4	SW1/5	SW1/6	SW1/7	SW1/8
0000h	On	On	On	On	On	On	On	On
0004h	On	On	On	On	On	On	On	On
0016h	On	On	On	On	On	On	On	On
0032h	On	On	On	On	On	On	On	On
0064h	On	On	On	On	On	On	On	On
FFACh	Off	Off	Off	Off	Off	Off	Off	Off
FFF0	Off	Off	Off	Off	Off	Off	Off	Off
FFF4	Off	Off	Off	Off	Off	Off	Off	Off
FFF8	Off	Off	Off	Off	Off	Off	Off	Off
FFFC	Off	Off	Off	Off	Off	Off	Off	Off

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BASE I/O ADDRESS SELECTION (CON'T)						
Setting	SW2/1	SW2/2	SW2/3	SW2/4	SW2/5	SW2/6
0000h	On	On	On	On	On	On
0004h	On	On	On	On	On	Off
0008h	On	On	On	On	Off	On
000Ch	On	On	On	On	Off	Off
0010	On	On	On	Off	On	On
FFECh	Off	Off	Off	On	Off	Off
FFF0h	Off	Off	Off	Off	On	On
FFF4h	Off	Off	Off	Off	On	Off
FFF8h	Off	Off	Off	Off	Off	On
FFFCh	Off	Off	Off	Off	Off	Off

Note: A total of 255 base address settings are available. The switches are a binary representation of the decimal memory addresses. SW1/1 is the Most Significant Bit and switch SW2/6 is the Least Significant Bit. The switches have the following decimal values: SW1/1=32768, SW1/2=16384, SW1/3=8192, SW1/4=4096, SW1/5=2048, SW1/6=1024, SW1/7=512, SW1/8=256, SW2/1=128, SW2/2=64, SW2/3=32, SW2/4=16, SW2/5=8, SW2/6=4 Turn off the switches and add the values of the switches to obtain the correct memory address.