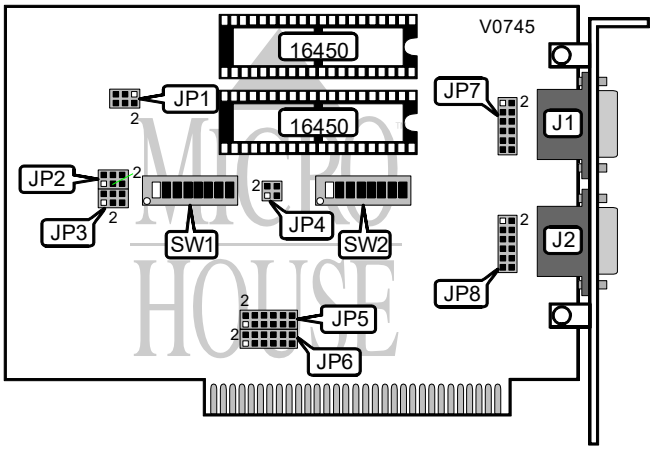
QUATECH, INC.
DS-102, DS-102S

Card Type Serial interface
Chipset Controller Unidentified
I/O Options Serial ports (2)
Maximum Dram N/A



CONNECTIONS			
Purpose	Location	Purpose	Location
Serial port 1	J1	Serial port 2	J2

SERIAL PORT CONFIGURATION		
Port 1	Port 2	JP4
Enabled	Enabled	Pins 1 & 2, 3 & 4 closed
Enabled	Disabled	Pins 1 & 2 closed
Disabled	Enabled	Pins 3 & 4 closed
Disabled	Disabled	Open

SERIAL INTERRUPT SHARING SELECTION			
Port 1	Port 2	P2	P3
Non-sharable	Non-sharable	Pins 2 & 3, 5 & 6 closed	Pins 2 & 3, 5 & 6 closed
Non-sharable	Sharable	Pins 2 & 3, 5 & 6 closed	Pins 1 & 2, 4 & 5 closed
Sharable	Non-sharable	Pins 1 & 2, 4 & 5 closed	Pins 2 & 3, 5 & 6 closed
Sharable	Sharable	Pins 1 & 2, 4 & 5 closed	Pins 1 & 2, 4 & 5 closed

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PORT 1 ADDRESS SELECT								
Address	SW1/1	SW1/2	SW1/3	SW1/4	SW1/5	SW1/6	SW1/7	SW1/8
000h	On	On	On	On	On	On	On	On
008h	On	On	On	On	On	On	On	Off
010h	On	On	On	On	On	On	Off	On
018h	On	On	On	On	On	On	Off	Off
2E8h (COM4:)	On	Off	On	Off	Off	Off	On	Off
2F8h (COM2:)	On	Off	On	Off	Off	Off	Off	Off
3E8h (COM3:)	On	Off	Off	Off	Off	Off	On	Off
3F8h (COM1:)	On	Off	Off	Off	Off	Off	Off	Off
7E0h	Off	Off	Off	Off	Off	Off	On	On
7E8h	Off	Off	Off	Off	Off	Off	On	Off
7F0h	Off	Off	Off	Off	Off	Off	Off	On
7F8h	Off	Off	Off	Off	Off	Off	Off	Off

Note: A total of 255 memory base address settings are available. The switches are a binary representation of the decimal addresses. Switch 8 is the Least Significant Bit and switch 1 is the Most Significant Bit. The switches have the following decimal values: switch 8=1, 7=2, 6=4, 5=8, 4=16, 3=32, 2=64, 1=128. Turn off the switches and add the off switches to obtain the correct memory base address. (On=0, Off=1)

PORT 2 ADDRESS SELECT								
Address	SW2/1	SW2/2	SW2/3	SW2/4	SW2/5	SW2/6	SW2/7	SW2/8
000h	On	On	On	On	On	On	On	On
008h	On	On	On	On	On	On	On	Off
010h	On	On	On	On	On	On	Off	On
018h	On	On	On	On	On	On	Off	Off
2E8h (COM4:)	On	Off	On	Off	Off	Off	On	Off
2F8h (COM2:)	On	Off	On	Off	Off	Off	Off	Off
3E8h (COM3:)	On	Off	Off	Off	Off	Off	On	Off
3F8h (COM1:)	On	Off	Off	Off	Off	Off	Off	Off
7E0h	Off	Off	Off	Off	Off	Off	On	On
7E8h	Off	Off	Off	Off	Off	Off	On	Off
7F0h	Off	Off	Off	Off	Off	Off	Off	On
7F8h	Off	Off	Off	Off	Off	Off	Off	Off

Note: A total of 255 memory base address settings are available. The switches are a binary representation of the decimal addresses. Switch 8 is the Least Significant Bit and switch 1 is the Most Significant Bit. The switches have the following decimal values: switch 8=1, 7=2, 6=4, 5=8, 4=16, 3=32, 2=64, 1=128. Turn off the switches and add the off switches to obtain the correct memory base address. (On=0, Off=1)

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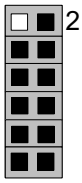
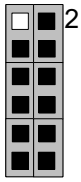
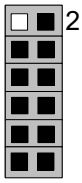
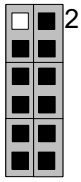
PORT 1 DTE/DCE SELECTION	
JP7	
DTE	**DCE**
	

PORT 2 DTE/DCE SELECTION	
JP8	
DTE	**DCE**
	

PORT 1 INTERRUPT SELECTION	
IRQ	**JP5**
2	Pins 1 & 2 closed
3	Pins 3 & 4 closed
4	Pins 5 & 6 closed
5	Pins 7 & 8 closed
6	Pins 9 & 10 closed
7	Pins 11 & 12 closed

PORT 2INTERRUPT SELECTION	
IRQ	**JP6**
2	Pins 1 & 2 closed
3	Pins 3 & 4 closed
4	Pins 5 & 6 closed
5	Pins 7 & 8 closed
6	Pins 9 & 10 closed
7	Pins 11 & 12 closed

INPUT CLOCK DIVISOR SELECT			
JP1			
10 (efault)	5	2	1