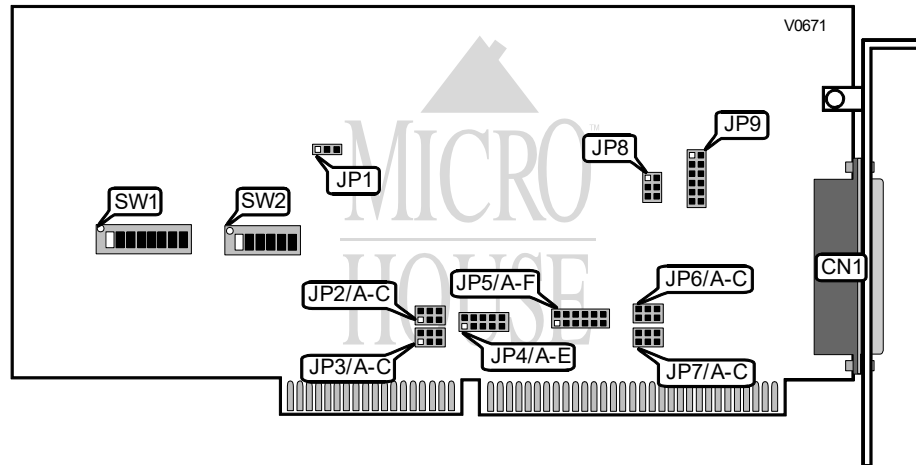


QUATECH, INC. PXB-160

Card Type	Parallel
Chipset Controller	Unidentified
I/O Options	Parallel ports (2)/Via proprietary cable
Maximum Dram	N/A



CONNECTIONS	
Purpose	Location
37-pin parallel port	CN1

STROBE WIDTH CONFIGURATION	
Setting	JP1
400 nano second	Pins 1 & 2 closed
100 nano second	Pins 2 & 3 closed

ADDRESS CONFIGURATION								
Address	SW1/1	SW1/2	SW1/3	SW1/4	SW1/5	SW1/6	SW1/7	SW1/8
0300h	On	On	On	On	On	On	Off	Off
02C8h	On	On	On	On	On	On	Off	On
3240h	On	On	Off	Off	On	On	Off	On

Note: The first set of switches are SW1/1 through SW1/8. The second set of switches are SW2/1 through SW2/5. The in the Off position switches are a binary representation of the addresses. The switches have the following decimal values: SW1/1 = 8, SW1/2 = 4, SW1/3 = 2, SW1/4 = 1; SW1/5 = 8, SW1/6 = 4, SW1/7 = 2, SW1/8 = 1; SW2/1 = 8, SW2/2 = 4, SW2/3 = 2, SW2/4 = 1; SW2/5 = 8. The switch in the on position is equal to 0.

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ADDRESS CONFIGURATION					
Address	SW2/1	SW2/2	SW2/3	SW2/4	SW2/5
0300h	On	On	On	On	On
02C8h	Off	Off	On	On	Off
3240h	On	Off	On	On	On
Note: The first set of switches are SW1/1 through SW1/8. The second set of switches are SW2/1 through SW2/5. The in the Off position switches are a binary representation of the addresses. The switches have the following decimal values: SW1/1 = 8, SW1/2 = 4, SW1/3 = 2, SW1/4 = 1; SW1/5 = 8, SW1/6 = 4, SW1/7 = 2, SW1/8 = 1; SW2/1 = 8, SW2/2 = 4, SW2/3 = 2, SW2/4 = 1; SW2/5 = 8. The switch in the on position is equal to 0.					




























BOARD SELECT	
Setting	SW2/6
Enabled	On
Disabled	Off

INTERRUPT CONFIGURATION					
IRQ	JP4/A	JP4/B	JP4/C	JP4/D	JP4/E
IRQ15	Closed	Open	Open	Open	Open
IRQ14	Open	Closed	Open	Open	Open
IRQ12	Open	Open	Closed	Open	Open
IRQ11	Open	Open	Open	Closed	Open
IRQ10	Open	Open	Open	Open	Closed

INTERRUPT CONFIGURATION (CONTINUED)						
IRQ	JP5/A	JP5/B	JP5/C	JP5/D	JP5/E	JP5/F
IRQ3	Closed	Open	Open	Open	Open	Open
IRQ4	Open	Closed	Open	Open	Open	Open
IRQ5	Open	Open	Closed	Open	Open	Open
IRQ6	Open	Open	Open	Closed	Open	Open
IRQ7	Open	Open	Open	Open	Closed	Open
IRQ9	Open	Open	Open	Open	Open	Closed

DMA CONFIGURATION						
IRQ	JP2/A	JP2/B	JP2/C	JP6/A	JP6/B	JP6/C
DACK1	Closed	Open	Open	Open	Open	Open
DACK2	Open	Closed	Open	Open	Open	Open
DACK3	Open	Open	Closed	Open	Open	Open
DACK5	Open	Open	Open	Closed	Open	Open
DACK6	Open	Open	Open	Open	Closed	Open
DACK7	Open	Open	Open	Open	Open	Closed

DRQ CONFIGURATION
Jumper JP9 & JP8

SINGLE BOARD CONFIGURATION				TWO BOARD CONFIGURATION							
JP9	OBF		CN1.30	JP9	OBF		CN1.30	JP9	OBF		CN1.30
	CN1.29		STB		CN1.29		STB		CN1.29		STB
	-XFER ACK		CN1.28		-XFER ACK		CN1.28		-XFER ACK		CN1.28
	CN1.27		-ACK		CN1.27		-ACK		CN1.27		-ACK
	DOUT		CN1.20		DOUT		CN1.20		DOUT		CN1.20
	CN1.21		DIN		CN1.21		DIN		CN1.21		DIN
				DTE					DCE		
JP8	TIMER2		CN1.36	JP8	TIMER2		CN1.36	JP8	TIMER2		CN1.36
	TIMER1		CN1.33		TIMER1		CN1.33		TIMER1		CN1.33
	IBF		CN1.25		IBF		CN1.25		IBF		CN1.25

Note: Under the two board communications connect JP8's Pins are all open.