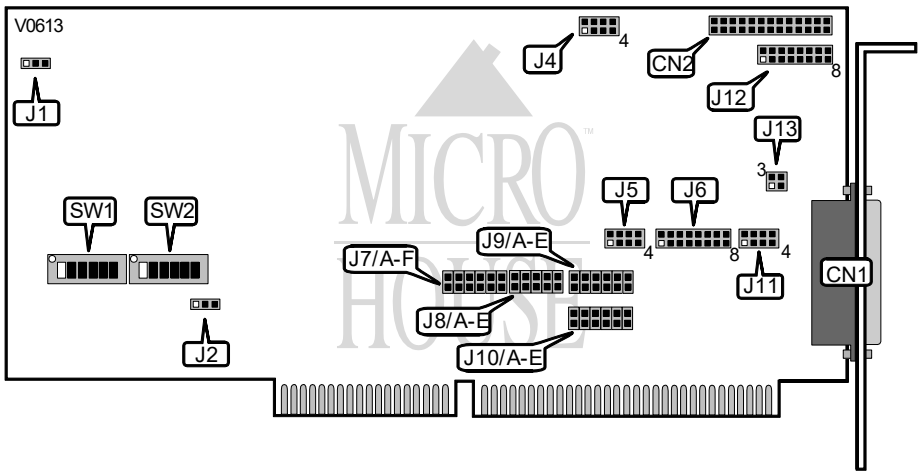
QUATECH, INC.
MPA-102

Card Type	Serial controller
Chipset/Controller	AMD
I/O Options	Serial ports (2)
Maximum DRAM	N/A



CONNECTIONS			
Purpos ɜ	Location	Purpos ɜ	Location
Serial port 1 - external DB-25	CN1	Serial port 2 - internal	CN2

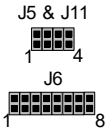
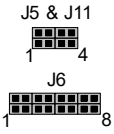
CLOCK SPEED	
Setting	J1
í 8MHz	pins 1 & 2 closed
6MHz	pins 2 & 3 closed

INTERRUPT SHARING	
Setting	J2
Interrupt sharing enabled	pins 1 & 2 closed
Interrupt sharing disabled	pins 2 & 3 closed

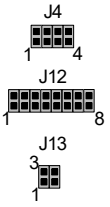
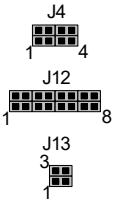
SERIAL PORT 1 (CN1) DTE/DCE SELECT			
Setting	J5	J6	J11
DTE configuration	pins 1 & 5, 2 & 6, 3 & 7, 4 & 8 closed	pins 1 & 9, 2 & 10, 3 & 11, 4 & 12, 5 & 13, 6 & 14, 7 & 15, 8 & 16 closed	pins 1 & 5, 2 & 6, 3 & 7, 4 & 8 closed
DCE configuration	pins 1 & 2, 3 & 4, 5 & 6, 7 & 8 closed	pins 1 & 2, 3 & 4, 5 & 6, 7 & 8, 9 & 10, 11 & 12, 13 & 14, 15 & 16 closed	pins 1 & 2, 3 & 4, 5 & 6, 7 & 8 closed

Continued on next page. . .

. . .continued from previous page

SERIAL PORT 1 (CN1) DTE/DCE SELECT	
DTE = 	DCE = 

SERIAL PORT 2 (CN2) DTE/DCE SELECT			
Setting	J4	J12	J13
DTE configuration	pins 1 & 5, 2 & 6, 3 & 7, 4 & 8 closed	pins 1 & 9, 2 & 10, 3 & 11, 4 & 12, 5 & 13, 6 & 14, 7 & 15, 8 & 16 closed	pins 1 & 3, 2 & 4 closed
DCE configuration	pins 1 & 2, 3 & 4, 5 & 6, 7 & 8 closed	pins 1 & 2, 3 & 4, 5 & 6, 7 & 8, 9 & 10, 11 & 12, 13 & 14, 15 & 16 closed	pins 1 & 2, 3 & 4 closed

DTE = 	DCE = 

INTERRUPT SELECT - J7 & J8											
IRQ	J7/A	J7/B	J7/C	J7/D	J7/E	J7/F	J8/A	J8/B	J8/C	J8/D	J8/E
IRQ2	closed	open	open	open	open	open	open	open	open	open	open
IRQ3	open	closed	open	open	open	open	open	open	open	open	open
IRQ4	open	open	closed	open	open	open	open	open	open	open	open
IRQ5	open	open	open	closed	open	open	open	open	open	open	open
IRQ6	open	open	open	open	closed	open	open	open	open	open	open
IRQ7	open	open	open	open	open	closed	open	open	open	open	open
IRQ10	open	open	open	open	open	open	closed	open	open	open	open
IRQ11	open	open	open	open	open	open	open	closed	open	open	open
IRQ12	open	open	open	open	open	open	open	open	closed	open	open
IRQ14	open	open	open	open	open	open	open	open	open	closed	open
IRQ15	open	open	open	open	open	open	open	open	open	open	closed

Continued on next page. . .

. . .continued from previous page

PORT 1 DMA SELECT - J9						
D lA Channel	Jumper A	Jumper B	Jumper C	Jumper D	Jumper E	Jumper F
Channel 1	closed	closed	open	open	open	open
Channel 2	open	open	closed	closed	open	open
Channel 3	open	open	open	open	closed	closed
Note: Channel selections are for both transmit and receive.						

PORT 2 DMA SELECT - J10						
D lA Channel	Jumper A	Jumper B	Jumper C	Jumper D	Jumper E	Jumper F
Channel 1	closed	closed	open	open	open	open
Channel 2	open	open	closed	closed	open	open
Channel 3	open	open	open	open	closed	closed
Note: Channel selections are for both transmit and receive.						

I/O ADDRESS CONFIGURATION		
Base Ad ress	SW1	SW2
300h	1, 2, 3, 4, 5 & 6 on	3, 4, 5 & 6 on
3F0h	1, 2, 3, 4, 5 & 6 on	all switches off
Note: The address range for the MPA-102 is from 0h to FFF0h. The switches are a binary representation of the addresses. When a switch is off, the corresponding bit is set to 1 and has the following decimal value: SW1/1=8, SW1/2=4, SW1/3=2, SW1/4=1, SW1/5=8, SW1/6=4, SW2/1=2. SW2/2=1, SW2/3=8, SW2/4=4, SW2/5=2, SW2/6=1. The MPA-102 requires 16 consecutive address locations.		