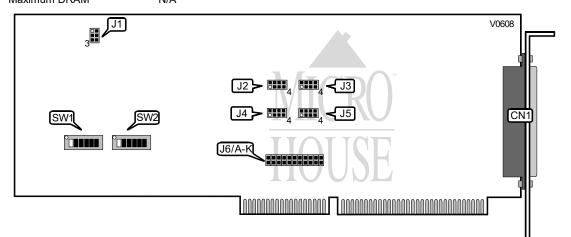
QUATECH, INC. QS-200D/DS, QS-300D/DS

Card Type Chipset/Controller I/O Options Maximum DRAM

Serial controller 16450/16550 UART Serial ports (4)



CONNECTIONS	
Purpose	Location
Serial ports (4) connector - DB-37	CN1
Note: CN1 can be converted to four DB-25 serial ports via a proprietary converter cable.	

CLOCK	SPEED
MHz	J1
í 1.8432MHz	pins 1 & 2, 4 & 5, 3 & 6 closed
3.6864MHz	pins 2 & 3, 4 & 5 closed
9.216MHz	pins 1 & 2, 5 & 6 closed
18.432MHz	pins 2 & 5 closed

SERIAL PORT 1 REQUEST TO SEND (RTS)/CLEAR TO SEND (CTS) MODE	
Setting	J2
í Loopback RTS to CTS	pins 1 & 5 closed
RTS transmit on AUXOUT/CTS receive on AUXIN	pins 1 & 2, 5 & 6 closed

SERIAL PORT 2 RTS/CTS MODE		RTS/CTS MODE
	Setting	J3
	í Loopback RTS to CTS	pins 1 & 5 closed
	RTS transmit on AUXOUT/CTS receive on AUXIN	pins 1 & 2, 5 & 6 closed

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SERIAL PORT 3 RTS/CTS MODE	
Setting J4	
í Loopback RTS to CTS	pins 1 & 5 closed
RTS transmit on AUXOUT/CTS receive on AUXIN	pins 1 & 2, 5 & 6 closed

SERIAL PORT 4 RTS/CTS MODE	
Setting	J5
í Loopback RTS to CTS	pins 1 & 5 closed
RTS transmit on AUXOUT/CTS receive on AUXIN	pins 1 & 2, 5 & 6 closed

SERIAL PORT 1 RCLK MODE	
Setting	J2
í Loopback XCLK to RCLK	pins 3 & 7 closed
Receive RCLK on AUXIN	pins 2 & 3 closed

SERIAL PORT 2 RCLK MODE	
Setting	J3
í Loopback XCLK to RCLK	pins 3 & 7 closed
Receive RCLK on AUXIN	pins 2 & 3 closed

SERIAL PORT 3 RCLK MODE Setting J4	
Receive RCLK on AUXIN	pins 2 & 3 closed

SERIAL PORT 4 RCLK MODE	
Setting	J5
í Loopback XCLK to RCLK	pins 3 & 7 closed
Receive RCLK on AUXIN	pins 2 & 3 closed

SERIAL PORT 1 XCLK MODE	
Setting	J2
í Loopback XCLK to RCLK	pins 3 & 7 closed
Transmit XCLK on AUXOUT	pins 6 & 7 closed

SERIAL PORT 2 XCLK MODE		2 XCLK MODE
	Setting	J3
	í Loopback XCLK to RCLK	pins 3 & 7 closed
	Transmit XCLK on AUXOUT	pins 6 & 7 closed

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SERIAL PORT	3 XCLK MODE		
Setting	J4		
í Loopback XCLK to RCLK	pins 3 & 7 closed		
Transmit XCLK on AUXOUT	pins 6 & 7 closed		

SERIAL PORT 4 XCLK MODE			
Setting	J5		
í Loopback XCLK to RCLK	pins 3 & 7 closed		
Transmit XCLK on AUXOUT	pins 6 & 7 closed		

SERIAL PORT 1 AUXIN/AUXOUT LOOPBACK			
Setting	J2		
í AUXIN/AUXOUT loopback enabled	pins 2 & 6 closed		
AUXIN/AUXOUT loopback disabled	pins 2 & 6 open		

SERIAL PORT 2 AUXIN/AUXOUT LOOPBACK			
Setting	J3		
í AUXIN/AUXOUT loopback enabled	pins 2 & 6 closed		
AUXIN/AUXOUT loopback disabled	pins 2 & 6 open		

SERIAL PORT 3 AUXIN/AUXOUT LOOPBACK			
Setting	J4		
í AUXIN/AUXOUT loopback enabled	pins 2 & 6 closed		
AUXIN/AUXOUT loopback disabled	pins 2 & 6 open		

SERIAL PORT 4 AUXIN/AUXOUT LOOPBACK			
Setting	J5		
í AUXIN/AUXOUT loopback enabled	pins 2 & 6 closed		
AUXIN/AUXOUT loopback disabled	pins 2 & 6 open		

SERIAL PORT 1 HALF/FULL DUPLEX SELECTION			
Setting	J2		
í Full-duplex mode enabled	pins 4 & 8 open		
Half-duplex mode enabled	pins 4 & 8 closed		

SERIAL PORT 2 HALF/FULL DUPLEX SELECTION			
Setting	J3		
í Full-duplex mode enabled	pins 4 & 8 open		
Half-duplex mode enabled	pins 4 & 8 closed		

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SERIAL PORT 3 HALF/FULL DUPLEX SELECTION			
Setting	J4		
í Full-duplex mode enabled	pins 4 & 8 open		
Half-duplex mode enabled	pins 4 & 8 closed		

SERIAL PORT 4 HALF/FULL DUPLEX SELECTION			
Setting	J5		
í Full-duplex mode enabled	pins 4 & 8 open		
Half-duplex mode enabled	pins 4 & 8 closed		

				INTERRI	JPT SFI	ECTION -	.J6				
IRQ	Α	В	С	D	Е	F	G	Н	I	J	K
í IRQ3	open	closed	open	open	open	open	open	open	open	open	open
IRQ2	closed	open	open	open	open	open	open	open	open	open	open
IRQ4	open	open	closed	open	open	open	open	open	open	open	open
IRQ5	open	open	open	closed	open	open	open	open	open	open	open
IRQ6	open	open	open	open	closed	open	open	open	open	open	open
IRQ7	open	open	open	open	open	closed	open	open	open	open	open
IRQ10	open	open	open	open	open	open	closed	open	open	open	open
IRQ11	open	open	open	open	open	open	open	closed	open	open	open
IRQ12	open	open	open	open	open	open	open	open	closed	open	open
IRQ14	open	open	open	open	open	open	open	open	open	closed	open
IRQ15	open	open	open	open	open	open	open	open	open	open	closed
Note: All po	orts share	the same	IRQ.	·		·	·				·

		I/O ADDRESS CONFIGURATION	
	Base Ad ress	SW1	SW2
	í 300h	1, 2, 3, 4, 5 & 6 on	3, 4 & 5 on
ĺ	54A0h	1, 3 & 5 on	1, 2 & 4 on

Note (1): The address range for the QS-200D/300D is from 0 to FFFFh. The switches are a binary representation of the addresses. When a switch is off, the corresponding bit is set to 1 and has the following decimal value: SW1/1=8, SW1/2=4, SW1/3=2, SW1/4=1, SW1/5=8, SW1/6=4, SW2/1=2, SW2/2=1, SW2/3=8, SW2/4=4, SW2/5=2. The QS-200D/300D requires 32 consecutive address locations for all four serial ports.

Note (2): The base address selected above is for Port 1. To obtain the addresses for the other ports, add to the Port 1 address the following numbers:

Port 2 address = Port 1 address + 8 Port 3 address = Port 1 address + 16 Port 4 address = Port 1 address + 24

INTERRUPT STATUS REGISTER	
Setting	SW2/6
í Scratchpad register enabled	Off
Interrupt status register enabled	On