# QUATECH, INC.
WSB-100 VER. 1

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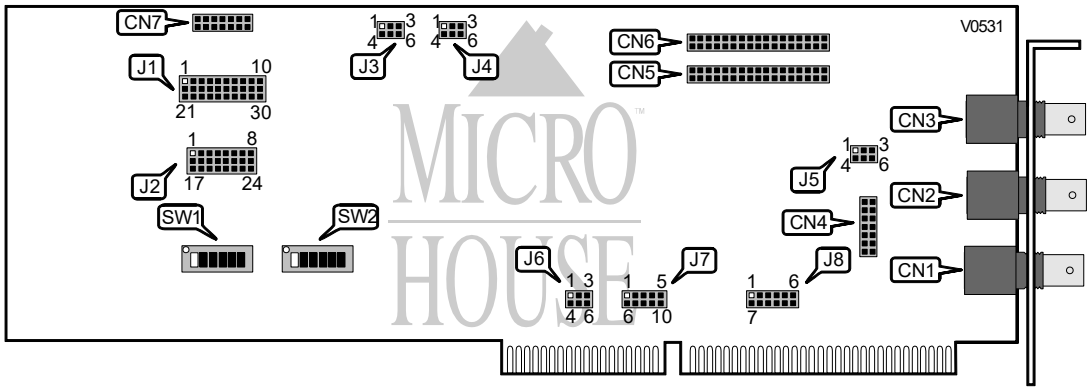
| **Card Type** | Waveform Synthesizer |
| **Chipset/Controller** | Intel |
| **I/O Options** | Analog/Clock/Digital/Strobe I/O ports |
| **Maximum DRAM** | N/A |




| CONNECTIONS | | | |
|---|---|---|---|
| Purpos ɜ | Location | Purpɔ ɜe | Location |
| Analog output | CN1 | Module signal connector | CN5 |
| Strobe/clock/trigger connector | CN2 | Multi-board data connector | CN6 |
| Strobe/clock/trigger connector | CN3 | Multi-board control connector | CN7 |
| Module power connector | CN4 | | |

| I/O ADDRESS CONFIGURATION | | |
|---|---|---|
| Addrɛ s | SW1 | SW2 |
| í 300h | 1, 2, 3, 4, 5 & 6 on | 3, 4, 5 & 6 on |
| 330h | 1, 2, 3, 4, 5 & 6 on | 3 & 4 |
| 2A60hh | 1, 2, 4 & 6 on | 2, 3 & 6 on |
| Note: The address range for the WSB-100 is from 0 to FFFFh. The switches are a binary representation of the addresses. The switches have the following decimal values: SW1/1=8, SW1/2=4, SW1/3=2, SW1/4=1, SW1/5=8, SW1/6=4, SW2/1=2, SW2/2=1, SW2/3=8, SW2/4=4, SW2/5=2, SW2/6=1, The DMM-100 requires sixteen consecutive address locations. | | |

| OPERATING MODE CONFIGURATION | | |
|---|---|---|
| lode | J1 | J2 |
| Single board system | 1 & 11, 2 & 12, 3 & 13, 4 & 14, 5 & 15, 6 & 16, 7 & 17, 8 & 18, 9 & 19, 10 & 20 closed | 1 & 9, 2 & 10, 3 & 11, 4 & 12, 5 & 13, 6 & 14, 7 & 15, 8 & 16 closed |

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| OPERATING MODE CONFIGURATION | | |
|---|---|---|
| lode | J1 | J2 |
| Single board system with delayed trigger | 1 & 11, 2 & 12, 3 & 13, 4 & 14, 5 & 15, 6 & 16, 7 & 17, 8 & 18, 9 & 19, 10 & 20 closed | 1 & 9, 2 & 10, 3 & 11, 4 & 12, 5 & 13, 14 & 22, 7 & 15, 8 & 16 closed |
| Simultaneous output - master board | 1 & 11, 2 & 12, 3 & 13, 4 & 14, 5 & 15, 6 & 16, 9 & 19, 10 & 20 closed 7, 17, 27, 8, 18 & 28 open | 9 & 17, 2 & 10, 3 & 11, 4 & 12, 5 & 13, 6 & 14, 15 & 23, 16 & 24 closed |
| Simultaneous output - slave board | 1 & 11, 12 & 22, 13 & 23,14 & 24, 15 & 25, 16 & 26, 19 & 29, 20 & 30 closed 7, 17, 27, 8, 18 & 28 open | 9 & 17, 2 & 10, 3 & 11, 4 & 12, 5 & 13, 6 & 14, 15 & 23, 8 & 16 closed |
| Master/slave mode - master board | 1 & 11, 2 & 12, 3 & 13, 4 & 14, 5 & 15, 6 & 16, 7 & 17, 8 & 18, 9 & 19, 10 & 20 closed | 9 & 17, 10 & 18, 11 & 19, 12 & 20, 5 & 13, 6 & 14, 7 & 15, 8 & 16 closed |
| Master/slave mode - slave board | 11 & 21, 12 & 22, 13 & 23, 14 & 24, 15 & 25, 16 & 26, 17 & 27, 18 & 28, 19 & 29, 20 & 30 closed | 9 & 17, 10 & 18, 11 & 19, 12 & 20, 5 & 13, 6 & 14, 7 & 15, 8 & 16 closed |
| Slave interrupting mode - master board | 1 & 11, 2 & 12, 3 & 13, 4 & 14, 5 & 15, 6 & 16, 7 & 17, 8 & 18, 9 & 19, 10 & 20 closed | 9 & 17, 2 & 10, 11 & 19, 4 & 12, 5 & 13, 6 & 14, 7 & 15, 8 & 16 closed |
| Slave interrupting mode - slave board | 1 & 11, 12 & 22, 13 & 23, 14 & 24, 15 & 25, 16 & 26, 17 & 27, 18 & 28, 19 & 29, 20 & 30 closed | 9 & 17, 2 & 10, 3 & 11, 4 & 12, 13 & 21, 6 & 14, 7 & 15, 8 & 16 closed |

| EXTERNAL CLOCK | | | |
|---|---|---|---|
| Sour e/Clock | J3 | J4 | J5 |
| CN2/clock 1 | pins 1 & 4 closed | N/A | pins 5 & 6 closed |
| CN3/clock 2 | N/A | pins 1 & 4 closed | pins 2 & 3 closed |

| TRIGGER SOURCE | | | |
|---|---|---|---|
| S urce | J3 | J4 | J5 |
| CN2 | pins 3 & 6 closed | N/A | pins 5 & 6 closed |
| CN3 | N/A | pins 3 & 6 closed | pins 2 & 3 closed |

| TRIGGER CLOCK | | | |
|---|---|---|---|
| S urce | J3 | J4 | J5 |
| CN2 | pins 2 & 5 closed | N/A | pins 5 & 6 closed |
| CN3 | N/A | pins 2 & 5 closed | pins 2 & 3 closed |

| CN2 I/O CONFIGURATION | | |
|---|---|---|
| I/O | J3 | J5 |
| Clock 1 input | pins 1 & 4 closed | pins 5 & 6 closed |
| Trigger delay clock input | pins 2 & 5 closed | pins 5 & 6 closed |

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| CN2 I/O CONFIGURATION | | |
|---|---|---|
| I/O | J3 | J5 |
| External trigger input | pins 3 & 6 closed | pins 5 & 6 closed |
| Data rate clock output | N/A | pins 4 & 5 closed |

| CN3 I/O CONFIGURATION | | |
|---|---|---|
| I/O | J4 | J5 |
| Clock 2 input | pins 1 & 4 closed | pins 2 & 3 closed |
| Trigger delay clock input | pins 2 & 5 closed | pins 2 & 3 closed |
| External trigger input | pins 3 & 6 closed | pins 2 & 3 closed |
| Data rate clock output | N/A | pins 1 & 2 closed |

| DMA SELECT | |
|---|---|
| Setting | J6 |
| í DMA 5 | pins 3 & 6 closed |
| DMA 6 | pins 2 & 5 closed |
| DMA 7 | pins 1 & 4 closed |

| INTERRUPT SELECT | | |
|---|---|---|
| IRQ | J7 | J8 |
| IRQ3 | N/A | pins 1 & 7 closed |
| IRQ4 | N/A | pins 2 & 8 closed |
| IRQ5 | N/A | pins 3 & 9 closed |
| IRQ6 | N/A | pins 4 & 10 closed |
| IRQ7 | N/A | pins 5 & 11 closed |
| IRQ9 | N/A | pins 6 & 12 closed |
| IRQ10 | pins 5 & 10 closed | N/A |
| IRQ11 | pins 4 & 9 closed | N/A |
| IRQ12 | pins 3 & 8 closed | N/A |
| IRQ14 | pins 2 & 7 closed | N/A |
| IRQ15 | pins 1 & 6 closed | N/A |