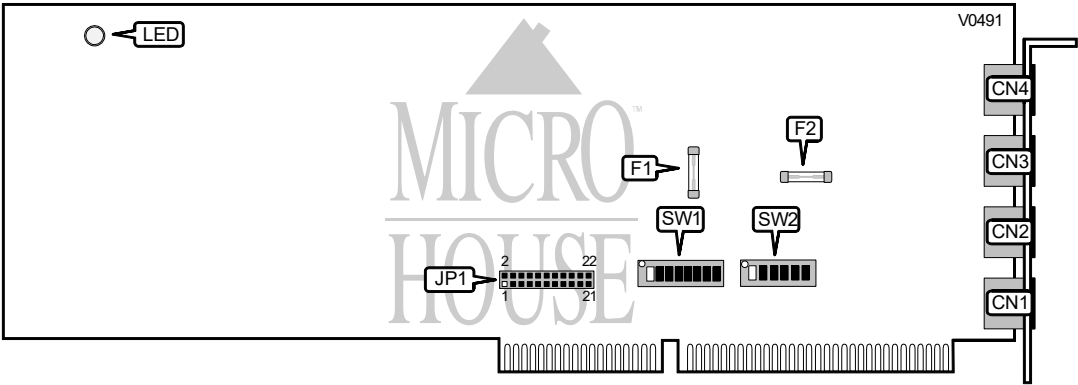


QUATECH, INC.
DDM-100

Card Type
Chipset/Controller
I/O Options
Maximum DRAM

Digital multi-meter adapter
Unidentified
Voltage, current, resistance and diode/continuity inputs
N/A



CONNECTIONS			
Purpose	Location	Purpose	Location
400mA range current test lead input	CN1	Ohmmeter test lead input	CN4
4A range current test lead input	CN2	5-amp fuse	F1
Common lead connector	CN3	5-amp fuse	F2

INTERRUPT SELECT	
IRQ	J1
IRQ Disabled	All Pins open
IRQ2	Pins 1 & 2 closed
IRQ3	Pins 3 & 4 closed
IRQ4	Pins 5 & 6 closed
IRQ5	Pins 7 & 8 closed
IRQ6	Pins 9 & 10 closed
IRQ7	Pins 11 & 12 closed
IRQ10	Pins 13 & 14 closed
IRQ11	Pins 15 & 16 closed
IRQ12	Pins 17 & 18 closed
IRQ14	Pins 19 & 20 closed
IRQ15	Pins 21 & 22 closed

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DMM-100

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I/O ADDRESS CONFIGURATION		
Address	SW1	SW2
0300h	1, 2, 3, 4, 5 & 6 on	1, 2, 3, 4, 5 & 6 on
0240h	1, 2, 3, 4, 5, 6 & 8 on	1, 3, 4, 5 & 6 on
06FC4h	1 & 4 on	3, 4 & 5 on
Note: The address range for the DMM-100 is from 0 to FFFFh. The switches are a binary representation of the addresses. The switches have the following decimal values: SW1/1=8, SW1/2=4, SW1/3=2, SW1/4=1, SW1/5=8, SW1/6=4, SW1/7=2, SW1/8=1, SW2/1=8, SW2/2=4, SW2/3=2, SW2/4=1, SW2/5=8, SW2/6=4. The DMM-100 requires four consecutive address locations.		