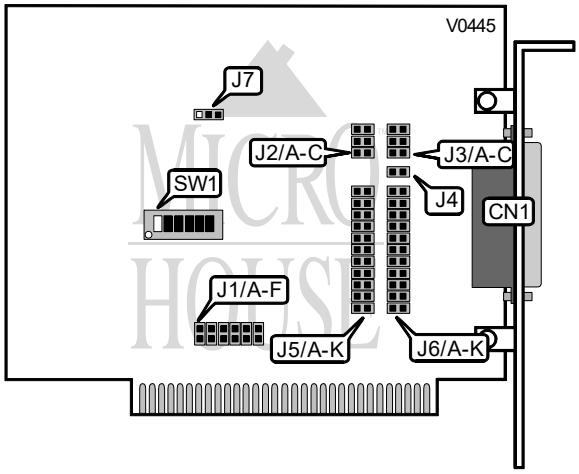
QUATECH, INC.
BCA-100

Card Type Serial/Parallel interface
Chipset/Controller Zilog
I/O Options Serial/Parallel port
Maximum DRAM N/A



CONNECTIONS			
Purpose	Location	Purpose	Location
DB-25 serial/parallel port	CN1	Standy clock output	J4

BASE MEMORY ADDRESS SELECT						
Address	SW1/1	SW1/2	SW1/3	SW1/4	SW1/5	SW1/6
27Xh	Off	On	On	Off	Off	Off
2EXh	Off	On	Off	Off	Off	On
2FXh	Off	On	Off	Off	Off	Off
37Xh	Off	Off	On	Off	Off	Off
3EXh	Off	Off	Off	Off	Off	On
3FXh	Off	Off	Off	Off	Off	Off

CLOCK SPEED SELECT	
Divide by	J7
1	Pins 1 & 2 closed
2	Pins 2 & 3 closed

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DTE/DCE CONFIGURATION		
Jumpe	J5 (DTI)	J6 (DCI)
A	On	Off
B	On	Off
C	On	Off
D	On	Off
E	On	Off
F	Off	Off
G	On	On
H	On	Off
I	Off	Off
J	On	Off
K	Off	Off

INTERRUPT SELECT						
IRQ	J1/A	J1/B	J1/C	J1/D	J1/E	J1/F
IRQ2	Closed	Open	Open	Open	Open	Open
IRQ3	Open	Closed	Open	Open	Open	Open
IRQ4	Open	Open	Closed	Open	Open	Open
IRQ5	Open	Open	Open	Closed	Open	Open
IRQ6	Open	Open	Open	Open	Closed	Open
IRQ7	Open	Open	Open	Open	Open	Closed

RECEIVE CLOCK SOURCE			
Sour e	J3/A	J3/B	J3/C
TXCA clock	On	Off	Off
RXCi external clock	Off	On	Off
CLKA	Off	Off	On

TRANSMIT CLOCK SOURCE			
Sour e	J2/A	J2/B	J2/C
RXCA clock	On	Off	Off
TXCi external clock	Off	On	Off
CLKB	Off	Off	On