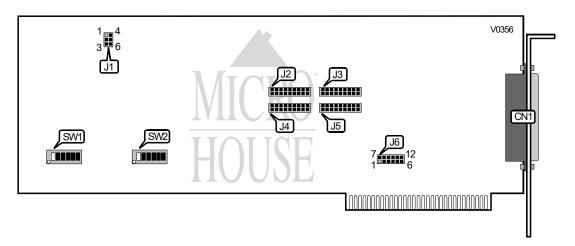
QUATECH, INC.

QS-100D, QS-100DS

Card Type
Chipset/Controller
I/O Options
Maximum DRAM

I/O controller Unidentified UART Serial ports (4)

Maximum DRAM N/A



CONNECTIONS	
Purpose	Location
DB-37 connector for serial ports (4)	CN1

CLOCK SPEED SELECT	
Speed	J1
í 18.432MHz	Pins 2 & 5 closed
9.612MHz	Pins 1 & 2, 5 & 6 closed
3.6864MHz	Pins 2 & 3, 4 & 5 closed
1.8432MHz	Pins 1 & 2, 3 & 6, 4 & 5 closed

	I/O ADDRESS CONFIGURATION	
Addres	SW1	SW2
300h	1 & 2, 3 & 4, 5 & 6 on	3 & 4, 5 on
06A0h	1 & 2, 3 & 4, 5 on	2 & 4 on
5220h	1 & 3, 5 & 6 on	2 & 3, 4 on

Note: The address range for the QS-100D is from 0 to FFFFh. The switches are a binary representation of the addresses. The switches have the following decimal values: SW1/1=8, SW1/2=4, SW1/3=2, SW1/4=1, SW1/5=8, SW1/6=4, SW2/1=2, SW2/2=8, SW2/3=4, SW2/4=2, SW2/5=1.

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INTERRUPT SELECT		
IRQ	J6	
IRQ2	Pins 1 & 7 closed	
IRQ3	Pins 2 & 8 closed	
IRQ4	Pins 3 & 9 closed	
IRQ5	Pins 4 & 10 closed	
IRQ6	Pins 5 & 11 closed	
IRQ7	Pins 6 & 12 closed	

INTERRUPT STATUS REGISTER CONFIGURATION	
Setting	SW2/6
Interrupt Status	On
Scratchpad	Off

SERIAL PORT DTE/DCE CONFIGURATION		
Serial Port 1	Serial Port 2	
Jumper J2	Jumper J3	
DCE DTE	DCE DTE	

SERIAL PORT DTE/DCE CONFIGURATION		
Serial Port 3	Serial Port 4	
Jumper J4	Jumper J5	
DCE DTE	DCE DTE	